REMARKS

The claims are claims 1, 4, 5, 9 to 11, 13, 16 and 17.

Claims 1, 4, 5, 10, 11 and 13 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Saishi et al U.S. Patent No. 6,167,419 and Pitsianis et al U.S. Patent Application Publication No. 2003/00088601. The OFFICE ACTION states that Saishi et al discloses rounding the combined product to form an intermediate result via an arithmetic circuit having a first input receiving first product, and a carry input to a mid-position receiving rounding value to form the intermediate result at elements 803, 806, and 807 in Figure 8 and column 8, lines 11 to 63.

Claims 1 and 13 recite further subject matter not made obvious by the combination of Saishi et al and Pitsianis et al. Claim 1 recites "a carry input to a mid-position receiving said rounding value to form the intermediate result." Claim 13 similarly recites "a mid-position carry input for mid-position rounding responsive to the rounding dot product instruction." Saishi et al fail to teach this use of a mid-position carry input for the recited rounding. Saishi et al states at column 8, lines 27 to 35 (within the portion cited in the OFFICE ACTION):

> "When the range indicated by the bit range 804 of the multiplication result 803 is desired to be cut out, and when it is assumed that the predetermined rounding position 811 is basically located at the mth bit from the least significant bit in consideration of the fact that a shift count required for a shift operation for cutting out is indicated by a right shift 809 of kbits, a signal having '1' at the (m+k)th bit is generated as the rounding signal. In other words, the rounding position is shifted to the left by k bits."

This clearly teaches that the rounding position is selected by the rounding generator generating a rounding signal shifted to

correspond to the later shift of the rounded product. One skilled in the art would understand the recited "shifter to the left by k bits" to be a multibit signal having 0's shifted into the k least significant bits to place a single 1 bit in the desired rounding position. Saishi et al never states that the rounding signal is input to "a carry input to a mid-position" as recited in claim 1 or to "a mid-position carry input" as recited in claim 13. The OFFICE ACTION fails to cite any portion of Saishi et al as making obvious the recited mid-position carry input. One skilled in the art would understand Saishi et al to teach supply of the rounding signal to an ordinary multi-bit data input of the adder. The left shifted 1 generated by the rounding signal generator is thus supplied to the data input and not to the carry input recited in claims 1 and 13. Thus Saishi et al teaches achieving the same result of this invention using a different method step or different apparatus. While the OFFICE ACTION states that this is disclosed in Saishi et al, in fact neither addition means 109, addition means 209, first subproduct addition means 306, first subproduct addition means 406, nor first subproduct addition means 506 illustrate the "carry input to a mid-position" recited in claim 1 and or the "mid-position carry input" recited in claim 13. The OFFICE ACTION does not allege that Pitsianis et al makes obvious this subject matter. Accordingly, claims 1 and 13 are not made obvious by the combination of Saishi et al and Pitsianis et al.

Claims 1 and 13 recite subject matter not made obvious by the combination of Saishi et al and Pitsianis et al. Claim 1 recites "combining the first product with the second product to form a combined product and rounding the combined product to form an intermediate result via an arithmetic circuit." Claim 13 similarly recites "an arithmetic circuit having a plurality of inputs each connected to receive a corresponding one of the plurality of products from the plurality of multipliers and a mid-position carry

input for mid-position rounding responsive to the rounding dot product instruction." The OFFICE ACTION states at page 3, lines 10 to 13 that Pitsianis et al discloses:

> "form a combined product (e.g. output of 625) and rounding (e.g. 627) the combined product to form an intermediate result via an arithmetic circuit (e.g. 627) having a first input receiving said first product, a second input receiving said second product."

The Applicants urge that the manner of rounding recited in claims 1 and 13 is unobvious over the manner of rounding disclosed in Pitsianis et al. Both claims 1 and 13 require the rounding to take place during the arithmetic combining of the two products. Claim 1 recites the rounding takes place "via an arithmetic circuit" during the combining of the first and second products. Claim 13 recites "an arithmetic circuit...for mid-position rounding." Pitsianis et al discloses at paragraph [0054]:

> "The selection of the bits and rounding occurs in selection and rounder circuit 627."

and at paragraph [0055]:

> "The results from adder 723 and subtractor 725 still need to be selected and rounded in selection and rounder circuit 727 and the final rounded results stored in the target register 729 in the CRF."

Pitsianis et al thus teaches that rounding takes place in selection and rounder circuit 627 or in selection and rounder circuit 727. The OFFICE ACTION cites adder 625 as making obvious the combining step of claim 1 and the adder circuit of claim 13. Thus the OFFICE ACTION states that Pitsianis et al teaches that the rounding takes place in a different method step (claim 1) or in a different structure (claim 13) than recited in the claims. The OFFICE ACTION

does not allege that Saishi et al makes obvious this subject matter. Accordingly, claims 1 and 13 are not made obvious by the combination of Saishi et al and Pitsianis et al.

Claim 10 recites subject matter not made obvious by the combination of Saishi et al and Pitsianis et al. Claim 10 recites "the step of combining comprises subtracting the product of second pair of elements from the product of first pair of elements." The OFFICE ACTION cites element 306 of Saishi et al as making obvious this subtraction. The Applicant respectfully submits that Saishi et al always refers element 306 as "first subproduct addition means," see: column 10, line 4; column 10, lines 6 and 7; column 10, lines 23 and 24; column 10, lines 29 and 30; column 10, lines 49 and 50; column 10, lines 50 and 51; and column 10, lines 65 and 66. Consistent reference to addition and no reference to subtraction fails to make obvious the subtraction recited in claim 10. The OFFICE ACTION does not allege that Pitsianis et al makes obvious this limitation. Accordingly, claim 10 is not made obvious by the combination of Saishi et al and Pitsianis et al.

Claims 4, 5 and 11 are allowable by dependence upon respective allowable base claims 1 and 13.

Claim 9 was rejected under 35 U.S.C. 103(a) as made obvious by the combination of Saishi et al. U.S. Patent No. 6,167,419, Pitsianis et al. U.S. Patent Application Publication No. 2003/00088601 and Slavenburg et al. U.S. Patent No. 5,963,744.

Claim 9 is allowable by dependence upon allowable claim 1.

Claims 16 and 17 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Saishi et al. U.S. Patent No. 6,167,419, Pitsianis et al. U.S. Patent Application Publication No. 2003/00088601 and Greggain et al. U.S. Patent No. 5,559,905.

Claims 16 and 17 are allowable by dependence upon respective allowable claims 1 and 13.

The application has been further amended at many locations to correct minor errors and to present uniform language throughout. The amendments include correction of those errors noted by the Examiner.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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